



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant

Paul A. Farrar et al.

BURIED CONDUCTORS

Docket No.: 303.367US3

Filed: November 11, 2003

Examiner: Ori Nadav

Serial No.: 10/705,185

Due Date: January 5, 2005

Group Art Unit: 2811

Mail Stop Amendment

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

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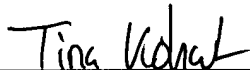
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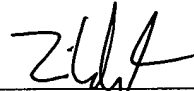
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 5 day of January, 2005.

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Signature



SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

(GENERAL)



JFW

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AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

MS Amendment
Commissioner for Patents
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REMARKS

This paper is in response to the Office Action mailed on October 5, 2004. Claims 1-21 are pending in this application.

Specification Objection

Applicant respectfully submits that the specification does provide enablement commensurate with the scope of Claims 1-2, 4, 8-9, 11-12, 15-16, 19-21 for at least the following reasons and respectfully requests that the objection be withdrawn.

Applicant's specification at page 4, lines 15-25 describes "Within N+ substrate 100 (i.e., doped silicon) are two buried conductive layers, layer 102 and layer 104. Layer 102 includes a series of conductive lines separated by an insulative material, where the conductive lines are parallel to the view shown in FIG. 1(a), such that only one such line is seen. Layer 104 includes a series of conductive lines also separated by an insulative material, but where the conductive lines are perpendicular to the view shown in FIG. 1(a), such that two such lines are seen. Layer 102 may thus be described as oriented in an x plane, and layer 104 oriented in a y plane. A conductive element may refer to either a layer within a semiconductor structure, or a conductive line within such a layer," as mentioned in Claim 1. Applicant further refers to Figs. 2(a), 2(b), 2(c), 2(f), 2(g) and Figs. 3 and 4. One of ordinary skill in the art upon reading the specification would find support for the claimed subject matter in the specification as a whole.

Applicant's specification at page 13, lines 19-21 describes "The melting point of the metal or alloy used should desirably be sufficiently high to prevent its melting or other unwanted metallurgical changes during further processing of the silicon," as mentioned in Claims 2 and 11.